WHAT IS CLAIMED IS:

1. A multiplexer circuit in a programmable logic device, said multiplier circuit having a circuit output and comprising:

N data inputs, where $N \geq 6$;

C control inputs; and

L look-up tables, each having only one table output, wherein:

$L = 0.5(N + MOD(N,2))$;

$C = L + 1$;

each of L - 2 of said L look-up tables has, as an input, a table output of another one of said L look-up tables, and has its table output directed only to an input of another one of said L look-up tables;

one of said L look-up tables other than said L - 2 look-up tables has its table output directed only to an input of one of said L - 2 look-up tables; and

another one of said L look-up tables, other than said L - 2 look-up tables and said one of said L look-up tables, has as an input the table output of one of said L - 2 look-up tables, the output of said another one of said L look-up tables being said circuit output.

2. The multiplexer circuit of claim 1 wherein each of said look-up tables has exactly four inputs.

3. The multiplexer circuit of claim 1 wherein:

at least some of said L look-up tables are adjacent one another; and

for at least some of said at least some of said L look-up tables, said table output is directed to an input of another of said at least some of said L look-up tables via a direct connection between said table output and said input of said another of said L look-up tables.

4. The multiplexer circuit of claim 3 wherein:

all of said L lookup tables are adjacent one another; and

for each of said L look-up tables other than said another one of said L look-up tables, said table output is directed to an input of another of said L look-up tables via a direct connection between said table output and said input of said another of said L look-up tables.

5. The multiplexer circuit of claim 1 wherein:

for at least some of said L look-up tables, said table output is directed to an input of another of said L look-up tables via a general interconnect resource of said programmable logic device.

6. The multiplexer circuit of claim 1 wherein:

each of said L look-up tables has as an input only one of said C control inputs, except for said one of said L look-up tables other than said L - 2 look-up tables, which also has as an input an extra one of said C control inputs; and

at any one time, only one of said C control inputs is in a first logic state, with each other of said C control inputs in a second logic state different from said first logic state, except for said extra one of said C control inputs which may be in either said first logic state or said second logic state.

7. The multiplexer circuit of claim 6 wherein at least one of said C control inputs is electrically inverted, with data in said look-up tables adjusted accordingly.

8. The multiplexer circuit of claim 1 wherein each said look-up table has four inputs.

9. A programmable logic device comprising the multiplexer circuit of claim 1.

10. A digital processing system comprising:

processing circuitry;

a memory coupled to said processing circuitry; and

a programmable logic device as defined in claim 9 coupled to the processing circuitry and the memory.

11. A printed circuit board on which is mounted a programmable logic device as defined in claim 9.

12. The printed circuit board defined in claim 11 further comprising:

memory circuitry mounted on the printed circuit board and coupled to the programmable logic device.

13. The printed circuit board defined in claim 12 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the memory circuitry.

14. An integrated circuit device comprising the multiplexer circuit of claim 1.

15. A digital processing system comprising:

processing circuitry;

a memory coupled to said processing circuitry; and

an integrated circuit device as defined in claim 14 coupled to the processing circuitry and the memory.

16. A printed circuit board on which is mounted an integrated circuit device as defined in claim 14.

17. The printed circuit board defined in claim 16 further comprising:

memory circuitry mounted on the printed circuit board and coupled to the integrated circuit device.

18. The printed circuit board defined in claim 17 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the memory circuitry.

19. A multiplexer circuit having a circuit output, N data inputs and C control inputs, and comprising L four-input look-up tables, each having only one table output, wherein $N \geq 6$, $L = 0.5(N + MOD(N,2))$ and $C = L + 1$; said L look-up tables comprising:

a first look-up table having, as inputs, two of said N data inputs and two of said C control inputs, said only one table output of said first look-up table being connected as input to a second look-up table;

an Lth look-up table having, as inputs, two of said N data inputs, one of said C control inputs and said only one table output of an (L - 1)th look-up table, said only one table output of said Lth look-up table being said circuit output; and

second through (L - 1)th look-up tables, each having, as inputs, two of said N data inputs, one of said C control inputs and a table output of another of said L look-up tables, said only one table output of each of said second through (L - 1)th look-up tables being an input to another of said L look-up tables.

20. The multiplexer circuit of claim 19 wherein:

at least some of said L look-up tables are adjacent one another; and

for at least some of said at least some of said L look-up tables, said table output is directed to an input of another of said at least some of said L look-up tables via a direct connection between said table output and said input of said another of said L look-up tables.

21. The multiplexer circuit of claim 20 wherein:

all of said L lookup tables are adjacent one another; and

for each of said first through (L - 1)th look-up tables, said table output is directed to an input of another of said L look-up tables via a direct connection between said table output and said input of said another of said L look-up tables.

22. The multiplexer circuit of claim 19 wherein:

each of said L look-up tables has as an input only one of said C control inputs, except for said first look-up table, which also has as an input an extra one of said C control inputs; and

at any one time, only one of said C control inputs is in a first logic state, with each other of said C control inputs in a second logic state different from said first logic state, except for said extra one of said C control inputs which may be in either said first logic state or said second logic state.

23. The multiplexer circuit of claim 19 wherein at least one of said C control inputs is electrically inverted, with data in said look-up tables adjusted accordingly.

24. A programmable logic device comprising the multiplexer circuit of claim 19.

25. A digital processing system comprising:

processing circuitry;

a memory coupled to said processing circuitry; and

a programmable logic device as defined in claim 24 coupled to the processing circuitry and the memory.

26. A printed circuit board on which is mounted a programmable logic device as defined in claim 24.

27. The printed circuit board defined in claim 26 further comprising:

memory circuitry mounted on the printed circuit board and coupled to the programmable logic device.

28. The printed circuit board defined in claim 27 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the memory circuitry.

29. An integrated circuit device comprising the multiplexer circuit of claim 19.

30. A digital processing system comprising:

processing circuitry;

a memory coupled to said processing circuitry; and

an integrated circuit device as defined in claim 29 coupled to the processing circuitry and the memory.

31. A printed circuit board on which is mounted an integrated circuit device as defined in claim 29.

32. The printed circuit board defined in claim 31 further comprising:

memory circuitry mounted on the printed circuit board and coupled to the integrated circuit device.

33. The printed circuit board defined in claim 32 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the memory circuitry.

34. A multiplexer circuit comprising:

L look-up tables;

a plurality of data inputs, each of said data inputs being connected to one of said L look-up tables; and

C control inputs; wherein:

C = L + 1.

35. The multiplexer circuit of claim 34 wherein:

each of said L look-up tables has as an input only one of said C control inputs, except for a first look-up table, which also has as an input an extra one of said C control inputs; and

at any one time, only one of said C control inputs is in a first logic state, with each other of said C control inputs in a second logic state different from said first logic state, except for said extra one of said C control inputs which may be in either said first logic state or said second logic state.

36. The multiplexer circuit of claim 35 wherein at least one of said C control inputs is electrically inverted, with data in said look-up tables adjusted accordingly.

37. A programmable logic device comprising the multiplexer circuit of claim 34.

38. A digital processing system comprising:

processing circuitry;

a memory coupled to said processing circuitry; and

a programmable logic device as defined in claim 37 coupled to the processing circuitry and the memory.

39. A printed circuit board on which is mounted a programmable logic device as defined in claim 37.

40. The printed circuit board defined in claim 39 further comprising:

memory circuitry mounted on the printed circuit board and coupled to the programmable logic device.

41. The printed circuit board defined in claim 40 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the memory circuitry.

42. An integrated circuit device comprising the multiplexer circuit of claim 34.

43. A digital processing system comprising:

processing circuitry;

a memory coupled to said processing circuitry; and

an integrated circuit device as defined in claim 42 coupled to the processing circuitry and the memory.

44. A printed circuit board on which is mounted an integrated circuit device as defined in claim 42.

45. The printed circuit board defined in claim 44 further comprising:

memory circuitry mounted on the printed circuit board and coupled to the integrated circuit device.

46. The printed circuit board defined in claim 45 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the memory circuitry.

47. A method for encoding control inputs of a multiplexer, said multiplexer comprising L interconnected look-up tables and having C said control inputs, said method comprising:

providing a respective one of said C control inputs to each of said L look-up tables;

providing another one of said C control inputs to only one of said L look-up tables, whereby C = L + 1; and

at any one time, asserting only one of said C control inputs in a first logic state, with each other of said C control inputs in a second logic state different from said first logic state, except for said second one of said C control inputs which may be in either said first logic state or said second logic state.

48. The method of claim 47 wherein said asserting comprises, at said any one time:

inverting at least one of said C control inputs; and

adjusting data in said look-up tables accordingly.

49. A method for encoding control inputs of a multiplexer having C said control inputs, said method comprising:

at any one time, asserting only one of a subset of all but a reserved one of said C control inputs in a first logic state, with each other of said subset of said control inputs being in a second logic state different from said first logic state; and

applying a signal to said reserved one of said C control inputs in either said first logic state or said second logic state.